Dual Very Low Noise Precision Operational Amplifier

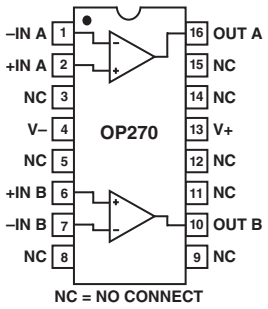
OP270

FEATURES

Very Low Noise 5 nV/√Hz @ 1 kHz Max
Excellent Input Offset Voltage 75 μV Max
Low Offset Voltage Drift 1 μV/°C Max
Very High Gain 1500 V/mV Min
Outstanding CMR 106 dB Min
Slew Rate 2.4 V/μs Typ
Gain Bandwidth Product 5 MHz Typ
Industry-Standard 8-Lead Dual Pinout

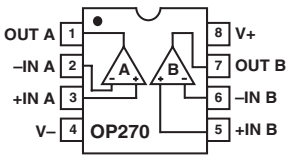
CONNECTION DIAGRAMS

16-Lead SOIC
(S-Suffix)



NC = NO CONNECT

8-Lead PDIP (P-Suffix)
8-Lead CERDIP
(Z-Suffix)



GENERAL DESCRIPTION

The OP270 is a high performance, monolithic, dual operational amplifier with exceptionally low voltage noise, 5 nV/√Hz max at 1 kHz. It offers comparable performance to ADI's industry standard OP27.

The OP270 features an input offset voltage below 75 μV and an offset drift under 1 μV/°C, guaranteed over the full military temperature range. Open-loop gain of the OP270 is over 1,500,000 into a 10 kΩ load, ensuring excellent gain accuracy and linearity, even in high gain applications. Input bias current is under 20 nA, which reduces errors due to signal source resistance. The OP270's CMR of over 106 dB and PSRR of less than 3.2 μV/V significantly reduce errors due to ground noise and power supply fluctuations. Power consumption of the dual OP270 is one-third less than two OP27s, a significant advantage for power conscious applications. The OP270 is unity-gain stable with a gain bandwidth product of 5 MHz and a slew rate of 2.4 V/μs.

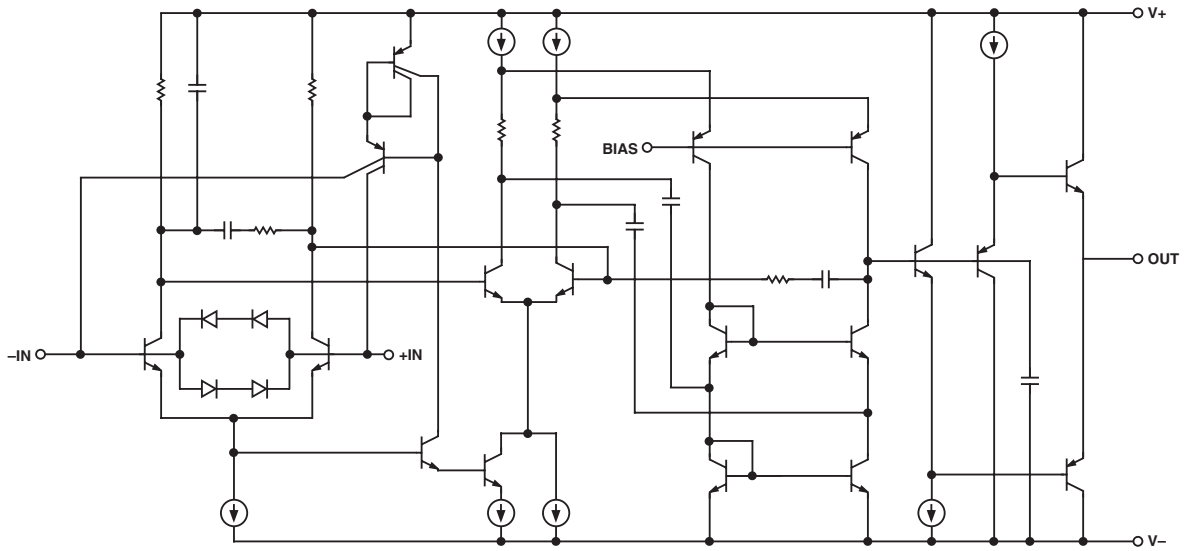
The OP270 offers excellent amplifier matching, which is important for applications such as multiple gain blocks, low noise instrumentation amplifiers, dual buffers, and low noise active filters.

The OP270 conforms to the industry-standard 8-lead DIP pinout. It is pin compatible with the MC1458, SE5532/A, RM4558, and HA5102 dual op amps, and can be used to upgrade systems using those devices.

For higher speed applications, the OP271, with a slew rate of 8 V/μs, is recommended. For a quad op amp, see the OP470.

SIMPLIFIED SCHEMATIC

(One of Two Amplifiers Is Shown)



OP270–SPECIFICATIONS (V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP270E			OP270F			OP270G			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V_{OS}			10	75		20	150		50	250	µV
Input Offset Current	l_{OS}	V_{CM} = 0 V		1	10		3	15		5	20	nA
Input Bias Current	I_B	V_{CM} = 0 V		5	20		10	40		15	60	nA
Input Noise Voltage	e_n p-p	0.1 Hz to 10 Hz (Note 1)		80	200		80	200		80		nV p-p
Input Noise Voltage Density		f_O = 10 Hz		3.6	6.5		3.6	6.5		3.6		nV/√Hz
		f_O = 100 Hz		3.2	5.5		3.2	5.5		3.2		nV/√Hz
	e_n	f_O = 1 kHz (Note 2)		3.2	5.0		3.2	5.0		3.2		nV/√Hz
Input Noise Current Density		f_O = 10 Hz		1.1			1.1			1.1		pA/√Hz
	i_n	f_O = 100 Hz		0.7			0.7			0.7		pA/√Hz
		f_O = 1 kHz		0.6			0.6			0.6		pA/√Hz
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ	1500	2300		1000	1700		750	1500		V/mV
		R_L = 2 kΩ	750	1200		500	900		350	700		V/mV
Input Voltage Range	IVR	(Note3)	±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	106	125		100	120		90	110		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.56	3.2		1.0	5.6		1.5	6	µV/V
Slew Rate	SR		1.7	2.4		1.7	2.4		1.7	2.4		V/µs
Supply Current (All Amplifiers)	I_{SY}	No Load		4	6.5		4	6.5		4	6.5	mA
Gain Bandwidth Product	GBP			5			5			5		MHz
Channel Separation	CS	V_O = ±20 V p-p f_O = 10 Hz (Note 1)	125	175		125	175			175		dB
Input Capacitance	C_{IN}			3			3			3		pF
Input Resistance Differential-Mode	R_{IN}			0.4			0.4			0.4		MΩ
Input Resistance Common-Mode	R_{INCM}			20			20			20		GΩ
Settling Time	t_S	A_V = +1, 10 V Step to 0.01%		5			5			5		µs

NOTES
1. Guaranteed but not 100% tested.
2. Sample tested.
3. Guaranteed by CMR test.

Specifications subject to change without notice.

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS (Vs = ±15 V, –40°C ≤ T_A ≤ 85°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	OP270E MIN	OP270E TYP	OP270E MAX	OP270F MIN	OP270F TYP	OP270F MAX	OP270G MIN	OP270G TYP	OP270G MAX	UNIT
Input Offset Voltage	V_{OS}			25	150		45	275		100	400	µV
Average Input Offset Voltage Drift	TCV_{OS}			0.2	1		0.4	2		0.7	3	µV/°C
Input Offset Current	I_{OS}	V_{CM} = 0 V		1.5	30		5	40		15	50	nA
Input Bias Voltage	I_B	V_{CM} = 0 V		6	60		15	70		19	80	nA
Large-Signal Voltage Gain	A_{VO}	V_O = ±10 V R_L = 10 kΩ	1000	1800		600	1400		400	1250		V/mV
		R_L = 2 kΩ	500	900		300	700		225	670		V/mV
Input Voltage Range*	IVR		±12	±12.5		±12	±12.5		±12	±12.5		V
Output Voltage Swing	V_O	R_L ≥ 2 kΩ	±12	±13.5		±12	±13.5		±12	±13.5		V
Common-Mode Rejection	CMR	V_{CM} = ±11 V	100	120		94	115		90	100		dB
Power Supply Rejection Ratio	PSRR	V_S = ±4.5 V to ±18 V		0.7	5.6		1.8	10		2.0	1.5	µV/V
Supply Current (All Amplifiers)	I_{SY}	No Load		4.4	7.2		4.4	7.2		4.4	7.2	mA

* Guaranteed by CMR test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±1.0 V
Differential Input Current[2] . . . . . ±25 mA
Input Voltage . . . . . Supply Voltage
Output Short-Circuit Duration . . . . . Continuous
Storage Temperature Range
P, S, Z Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
Junction Temperature (T_J) . . . . . –65°C to +150°C
Operating Temperature Range
OP270E, OP270F, OP270G . . . . . –40°C to +85°C

NOTES

[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2] The OP270's inputs are protected by back-to-back diodes. Current limiting resistors are not used, in order to achieve low noise performance. If differential voltage exceeds +10 V, the input current should be limited to ±25 mA.

ORDERING GUIDE

Model	T_A = +25°C V_{OS} Max (μV)	θ_{JC} (°C/W)	θ_{JA}* (°C/W)	Temperature Range	Package Description	Package Option
OP270EZ	75	12	134	XIND	8-Lead CERDIP	Q-8 (Z-Suffix)
OP270FZ	150	12	134	XIND	8-Lead CERDIP	Q-8 (Z-Suffix)
OP270GP	250	37	96	XIND	8-Lead PDIP	N-8 (P-Suffix)
OP270GS	250	27	92	XIND	16-Lead SOIC	RW-16 (S-Suffix)

*θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for CERDIP and PDIP packages; θ_{JA} is specified for device soldered to printed circuit board for SOIC package.

For military processed devices, please refer to the Standard Microcircuit Drawing (SMD) available at www.dscc.dla.mil/programs/milspec/default.asp.

SMD Part Number	ADI Equivalent
5962-8872101PA	OP270AZMDA

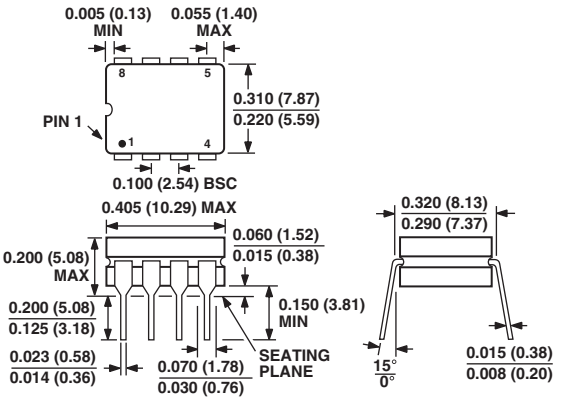
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP270 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

OUTLINE DIMENSIONS

8-Lead Ceramic Dual In-Line Package [CERDIP]
Z-Suffix
(Q-8)

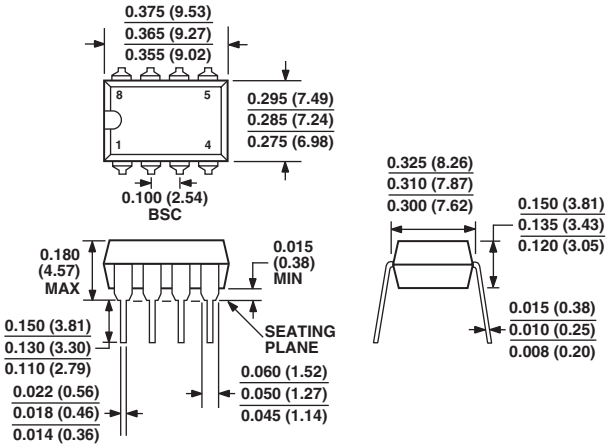
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Plastic Dual In-Line Package [PDIP]
P-Suffix
(N-8)

Dimensions shown in inches and (millimeters)

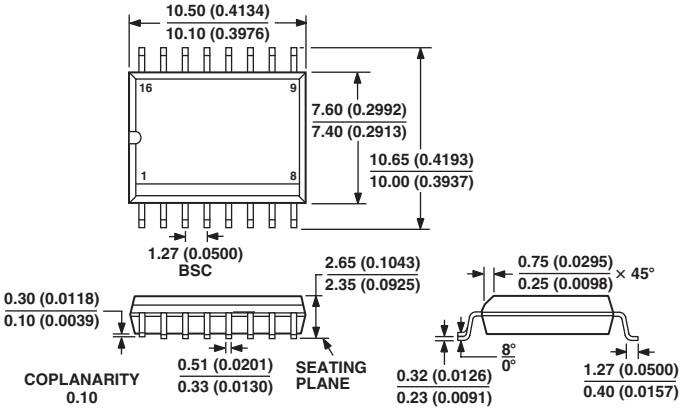


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Standard Small Outline Package [SOIC]
Wide Body
S-Suffix
(RW-16)

Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-013AA

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